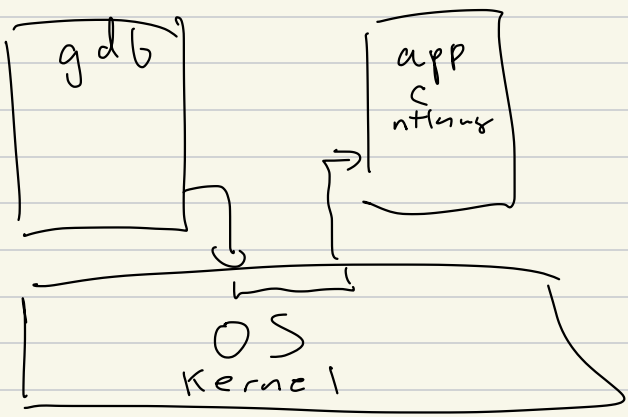
CS631-01 Debugging 2026-02-24

Project01 Q&A

Debuggers



RISC-V Assembly — Instruction set Architecture (ISA)

instructions
add sub

registers
add t0, t1, t2 t0 = t1 + t2
registers processor scribbles.

RISC-V 64 bit word / pointer is 64 bits

memory / stack

program:

labels → add3:
```
add a0, a0, a1
add a0, a0, a2
ret
```

function

```
int add2(int x, int y, int z)
{
  return x+y+z;
}
```